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18EC34

Third Semester B.E. Degree Examination, July/August 2022
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Convert the following Boolean function into minterm canonical or maxterm canonical form:
(i) $y = \bar{\omega}x + y\bar{z}$ (ii) $(A+\bar{B}+C)(\bar{A}+D)$ **(06 Marks)**

b. Simplify the Boolean function and identify the prime and essential prime implicants:
(i) $f(a,b,c,d) = \sum m\,(1, 5, 7, 8, 9, 10, 11, 13, 15)$
(ii) $f(a,b,c,d) = \pi M\,(0, 2, 3, 8, 9, 10, 12, 14)$ **(06 Marks)**

c. Simplify the given Boolean function using Quine-Mc Cluskey method.
$f(a,b,c,d) = \sum m\,(0, 1, 2, 3, 6, 7, 8, 9, 14, 15)$ **(08 Marks)**

OR

2 a. Design a combinational logic circuit that has three input variables and produces a logic 1 output when more than one input variables are logic 1. **(06 Marks)**

b. Simplify the following Boolean function using K-map.
(i) $f(w,x,y,z) = \pi(2, 3, 8, 9, 10, 11, 12, 13, 14, 15)$
(ii) $f(w,x,y,z) = \sum m\,(6, 7, 9, 10, 13) + \sum d\,(1, 4, 5, 11, 15)$ **(06 Marks)**

c. Simplify the given Boolean function using Quine-Mc Clusky method.
$f(w,x,y,z) = \sum m(1,3,13,15) + \sum d(8,9,10,11)$ **(08 Marks)**

Module-2

3 a. Design a combinational circuit using 3 : 8 decoder (IC – 74138) that generates a logic 1 output when majority of 4 inputs are true. **(06 Marks)**

b. Explain 4-bit carry look ahead adder with neat diagram. **(08 Marks)**

c. Implement a full adder using PAL. **(06 Marks)**

OR

4 a. Implement $f(w,x,y,z) = \sum m(0,1,2,4,5,7,8,9,12,13)$ using 8 : 1 MUX with w,x,y as select lines. **(06 Marks)**

b. Design 2-bit magnitude comparator. **(08 Marks)**

c. Explain the Basic Architecture of a Xilinx XCR3064XL CPLD. **(06 Marks)**

Module-3

5 a. Explain the working of Master Slave JK Flip-Flop with function table and timing diagram. **(08 Marks)**

b. Differentiate between Flip Flops and Latches. **(04 Marks)**

c. Design an universal shift Register using positive edge triggered DFF having the behavior as specified.

Mode	Operation
00	Hold
01	Shift right
10	Shift left
11	Parallel load

(08 Marks)

OR

6 a. Explain positive edge Triggered D Flip Flop with the help of circuit diagram and waveform. **(08 Marks)**

b. Obtain the characteristic equation for the following Flip Flop (i) J.K. (ii) S.R. **(06 Marks)**

c. Design a mod-8 asynchronous upcounter using negative edge triggered JK FF. **(06 Marks)**

Module-4

7 a. Design a synchronous mod-6 counter using clocked JK Flip Flop for the sequence $0-2-3-6-5-1$ **(08 Marks)**

b. Distinguish between Moore and Melay model with necessary block diagram. **(06 Marks)**

c. Analyze the following synchronous circuit. (Refer Fig. Q7 (c))

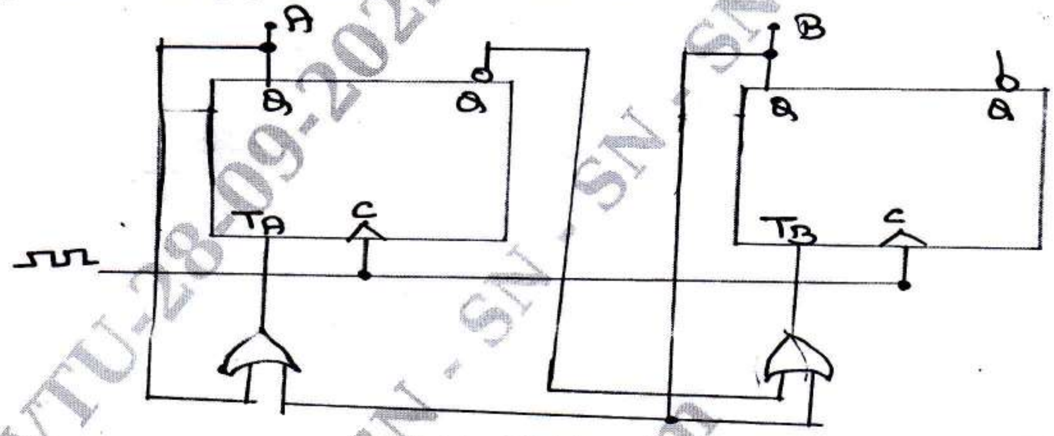

Fig. Q7 (c) **(06 Marks)**

OR

8 a. Design a synchronous mod-6 counter using clocked T-Flip Flop for the sequence, $0-2-3-6-5-1$. **(06 Marks)**

b. Draw the state diagram, for the sequential circuit shown. (Refer Fig. Q8 (b))

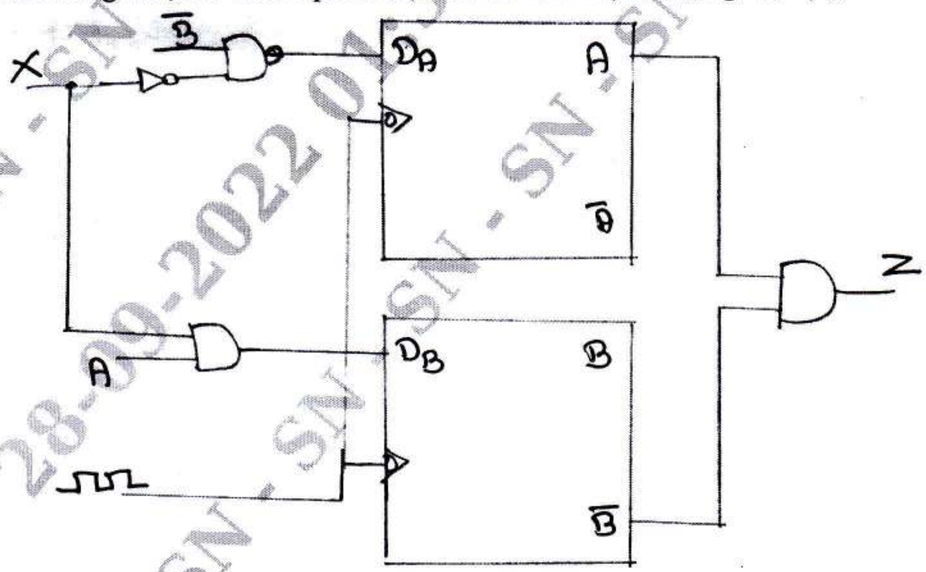

Fig. Q8 (b) **(06 Marks)**

c. Analyze the given synchronous sequential circuit. (Refer Fig. Q8 (c))

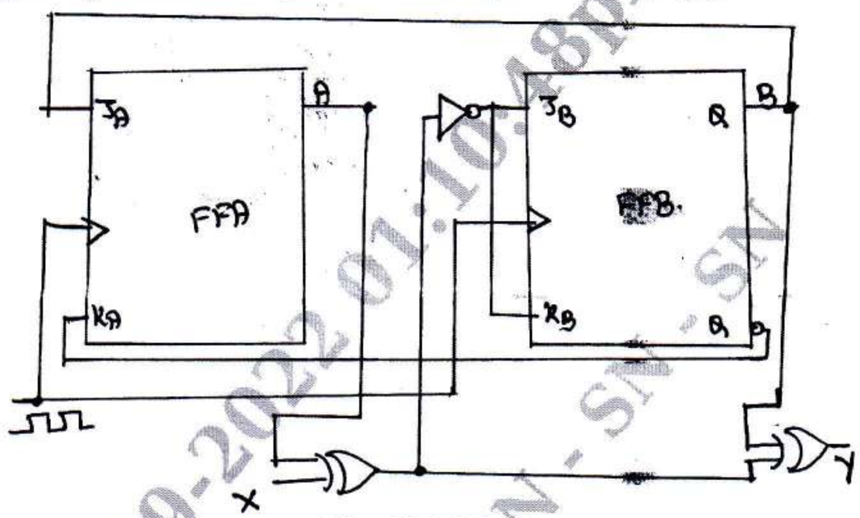

Fig. Q8 (c) **(08 Marks)**

Module-5

9 a. Design a Mealy type sequence detector to detect a serial input sequence of 101. **(08 Marks)**
b. List the guidelines for construction of state graphs. **(06 Marks)**
c. With the help of neat block diagram, explain serial adder with accumulator. **(06 Marks)**

OR

10 a. Design a Moore type sequence detector to detect a serial input sequence of 101. **(08 Marks)**
b. Construct Moore and Mealy state diagram, that will detect input sequence 10110, when input pattern is detected, z is asserted high. Give state diagrams for each state. **(06 Marks)**
c. With the help of neat block diagram, explain parallel binary divider. **(06 Marks)**

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